Appl. No. 10/615,918 Amdt. Dated 02/10/2005 Reply to Office Action of 11/10/2004

Appendix 2

ANNOTATED FORMAL DRAWING SHEET AMENDED FIGURE 7

Docket No: 42P7098C WEA//tn

Stall for Next to Last PipeStage (NLP)

Stall (NLP) = Valid Instruction in Pipe(NLP) AND (ThreadId <math>(NLP) = ThreadId of Stall)

Stall for any other PipeStageX

 $Stall_{(X)} = Valid\ Instruction\ in\ Pipe_{(X)}\ AND\ Valid\ Instruction\ in\ Pipe_{(X+1)}\ AND\ Stall_{(NLP)}$

Powerdown for any PipeStage X

Powerdown_(X) = NOT Valid Instruction in Pipe_(X-1)

Clock Enable for any PipeStage X

 $Clock(\chi) = NOT Stall(\chi) AND NOT Powerdown(\chi)$

Clock for any PipeStage X

NOT Clock_(X) AND [(ClearThread(Id₀) AND (ThreadId_(X) = Id₀)) OR (ClearThread(Id₁) AND (ThreadId_(X) = Id₁))] $Clear(\chi) = Clock(\chi) \ AND \ [(ClearThread(Id0) \ AND \ (ThreadId(\chi_{-1}) = Id0)) \ OR \ (ClearThread(Id1) \ AND \ (ThreadId(\chi_{-1}) = Id1))]$

ClearThread (140) = There was a Clear on Thread Identification 0

ClearThread (1d1) = There was a Clear on Thread Identification 1

Pipe(X) = Any pipestage in the decode

Pipe(X-1) = Pipestage before Pipe(X)

Pipe(X+1) = Pipestage after Pipe(X)

FIG. 7